In the Claims:

Please amend the claims as follows:

1. (Cancelled)

2. (Currently Amended) A process for forming trenches with an oblique profile and rounded top corners, comprising the steps of:

through a first polymerizing etch, forming in a semiconductor wafer depressions delimited by rounded top corners; ~~and~~

through a second polymerizing etch, opening trenches at said depressions;

applying a wafer voltage to the semiconductor wafer;

wherein said second polymerizing etch is performed by controlling plasma conditions around the semiconductor wafer to form trenches with oblique profiles having a substantially constant slope throughout substantially an entire sidewall of each trench, and wherein controlling the plasma conditions includes controlling the wafer voltage applied to the semiconductor wafer to thereby control an etching voltage between a plasma around the wafer and said wafer.

3. (Previously Presented) The process according to claim 2, wherein said step of controlling comprises increasing said etching voltage.

4. (Previously Presented) The process according to claim 2, wherein said etching voltage is a discrete-ramp voltage.

5. (Previously Presented) The process according to claim 4, wherein said etching voltage has steps of constant duration.

6. (Previously Presented) The process according to claim 5, wherein said constant duration is approximately 30 seconds.

7. (Withdrawn) The process according to claim 2, characterized in that said etching voltage is a linear-ramp voltage.

8. (Previously Presented) The process according to claim 2, wherein said step of controlling said etching voltage comprises:

placing said wafer in an etching chamber;

supplying to said etching chamber a constant chamber voltage; and

supplying to said wafer a variable wafer voltage.

9. (Previously Presented) The process according to claim 2, wherein said second polymerizing etch is an HBr- and O_2-based etch.

10. (Previously Presented) The process according to claim 9, wherein said second polymerizing etch is made in the presence of Cl_2 and N_2.

11. (Previously Presented) The process according to claim 2, wherein said first polymerizing etch is made using a substance chosen from the group comprising CHF_3, CH_2F_2.

12. (Withdrawn) The process according to claim 1, characterized in that said step of forming said second polymerizing etch comprises increasing a concentration of a polymerizing species present in said plasma.

13. (Withdrawn) The process according to claim 1, characterized in that said step of forming said second polymerizing etch comprises increasing a pressure of said plasma.

14. (Previously Presented) The process according to claim 2, wherein said step of forming a first polymerizing etch and said step of forming a second polymerizing etch are performed using a masking structure.

15. (Previously Presented) The process according to claim 2, wherein the process comprises the step of filling said trench with a dielectric material.

16. (Withdrawn) A semiconductor wafer comprising active areas and trenches defining said active areas; characterized in that said trenches have rounded top corners and are delimited by oblique walls having constant slope.

17. (Withdrawn) The wafer according to claim 16, characterized in that said constant slope is between 65° and 85°.

18. (Withdrawn) The wafer according to claim 16, characterized in that said trenches are filled with dielectric material, thereby forming insulating structures.

19-21. (Cancelled)

22. (Previously Presented) The method of claim 24 wherein the first plasma etch further comprises etching with a CHF_3 based plasma.

23. (Withdrawn) The method of claim 20 wherein the second plasma etch further comprises etching with a variable anisotropic plasma.

24. (Previously Presented) A method, comprising:

forming a trench in an unmasked area of a substrate, the trench having inclined walls with a substantially constant slope and with rounded top corners; and

filling the trench with a dielectric material;

wherein forming the trench further comprises:

performing a first plasma etch; and

performing a second plasma etch; and

wherein the first plasma etch further comprises:

forming a depression in the unmasked area of the substrate, wherein the depression is formed through a stop layer formed over the substrate and a resist layer formed on the stop layer; and

forming a first polymeric film on walls defined by the depression, stop layer, and resist layer; and

wherein the second plasma etch further comprises:

placing a wafer in a chamber, the wafer including the substrate;

filling the chamber with a second plasma mixture of gases;

setting the temperature, pressure and gas flow;

setting a chamber voltage;

setting a series of substrate voltages;

creating a series of etching voltages between the substrate and the second plasma mixture of gases;

removing portions of the substrate in series, each portion being removed responsive to one of the etching voltages in the series of etching voltages; and

depositing portions of a second polymeric film on the walls in series, each portion in the series of deposited portions being deposited responsive to one of the etching voltages in the series of etching voltages.

25. (Original) The method of claim 24 wherein the plasma mixture of gases further comprises mixing hydrogen bromide and oxygen.

26. (Original) The method of claim 24 wherein the plasma mixture of gases further comprises mixing chlorine and nitrogen.

27. (Original) The method of claim 24 wherein a rate of depositing the second polymeric film increases as the absolute value of the etching voltages increase.

28. (Original) The method of claim 24 wherein depositing the second polymeric film further comprises controlling the growth of the walls of the trench by the series of etching voltages.

29. (Original) The method of claim 24 wherein creating a series of wafer voltages further comprises:

setting the wafer voltage to 10 volts for a first thirty seconds;

setting the wafer voltage to 20 volts for a second subsequent thirty seconds; and

setting the wafer voltage to 30 volts for a third subsequent thirty seconds.

30. (Original) The method of claim 24 wherein removing portions of the wafer by parts in series further comprises:

exposing decreasing portions of the wafer; and

keeping a slope of the walls of the trench substantially constant.

31. (Original) The method of claim 30 wherein the slope the walls is at an angle between sixty-five and eighty-five degrees to a vertical.

32. (Previously Presented) The method of claim 24 wherein filling the trench with a dielectric material further comprises chemical-vapour deposition.

33. (Original) The method of claim 32, further comprising depositing silicon oxide.

34. (Withdrawn) The method of claim 24 wherein creating a series of etching voltages further comprises continuously varying a voltage in a linear manner.

35. (Withdrawn) The method of claim 24 wherein setting the gas flow further comprises:

etching the wafer with a first gas;

depositing a second polymeric film with a second gas;

varying the concentration of the second gas; and

controlling the rate of polymerization.

36. (Withdrawn) The method of claim 35, further comprising:

etching the wafer with hydrogen bromide; and

depositing the second polymeric film with helium oxide.

37. (Withdrawn) The method of claim 35, further comprising:

etching the wafer with hydrogen bromide; and

depositing the second polymeric film with oxygen.

38. (Withdrawn) The method of claim 35, further comprising:
etching the wafer with chlorine; and
depositing the second polymeric film with nitrogen.

39. (Withdrawn) The method of claim 35, further comprising varying the concentration of the second gas according to a discrete-ramp pattern.

40. (Withdrawn) The method of claim 24 wherein setting the pressure further comprises varying the pressure according to a discrete-ramp pattern during the second plasma etch.

41. (Original) The method of claim 24 wherein creating a series of etching voltages further comprises a non-uniform voltage step function.

42. (Original) The method of claim 24 wherein creating a series of etching voltages further comprises a discrete parabolic voltage function.

43. (Original) The method of claim 24 wherein creating a series of etching voltages further comprises a continuous parabolic voltage function.

44. (Original) The method of claim 24 wherein the steps have different durations.

45. (Cancelled)

46. (Currently Amended) A method for forming trenches with an oblique profile and rounded top corners in a wafer, comprising:

forming depressions delimited by rounded top corners in a wafer with a first polymerizing etch;

applying a wafer voltage to the semiconductor wafer; and

forming trenches at the depressions with a varying plasma polymerizing etch, the oblique profile of each trench having approximately a same constant angle relative to a surface parallel to a face of the wafer, wherein forming trenches further comprises controlling an etching voltage between a plasma around the wafer and the wafer by varying the wafer voltage applied to the semiconductor wafer.

47. (Previously Presented) The method of claim 46 wherein controlling an etching voltage further comprises increasing the etching voltage.

48. (Original) The method of claim 47 wherein increasing the etching voltage further comprises a discrete-ramp voltage function.

49. (Original) The method of claim 48 wherein the discrete-ramp voltage function further comprises steps of constant duration.

50. (Withdrawn) A micro-electric insulating structure, comprising:

a trench in a substrate with inclined walls having a substantially constant slope and with rounded top corners; and

a dielectric material disposed in the trench.

51. (Withdrawn) The structure of claim 50 wherein the substantially constant slope is between sixty-five degrees and eighty-five degrees.

52. (Withdrawn) An electronic component, comprising:

micro-electric insulating structures, comprising:

trenches in a substrate with inclined walls having a substantially constant slope and with rounded top corners; and

a dielectric material disposed in the trenches; and

active micro-electric structures between the micro-electric insulating structures.

53. (Withdrawn) An integrated circuit, comprising:

electronic components, comprising:

micro-electric insulating structures, comprising:

trenches in a substrate with inclined walls having a substantially constant slope and with rounded top corners; and

a dielectric material disposed in the trenches; and

active micro-electric structures between the micro-electric insulating structures; and

electronic connectors between the electronic components.